Oral S07

High Speed Clocking Interface

Date/Venue	8/7 (四)11:10-12:10 · [8F 皇愉會議室 8-1A]
Chair(s)	劉仁傑 國立聯合大學電機工程學系、林群祐 國立陽明交通大學電子研究所

S07.1

A 2.9-Gb/s Transceiver Using Phase Interpolation for Spread-Spectrum-Modulation Chip-to-Chip Links

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To reduce peak electromagnetic emissions and comply with EMI regulations required for systems with high-speed interconnects, this work presents a fully integrated 2.9-Gb/s transceiver using spread-spectrum clocking (SSC) with a 45.8 kHz modulation frequency and -1.5% modulation depth. The PLL generates 2.9-GHz 4-phase clocks for the transmitter, which applies SSC through a phase-interpolating technique to modulate the clock and drive the data. On the receiver side, 725-MHz 4-phase clocks are used along with the same phase-interpolating method for clock recovery in the timing recovery loop. Fabricated in a 90-nm CMOS process, the transceiver consumes 53 mW and achieves more than 24 dB EMI attenuation.

S07.2

An 80-GHz Triple-Band VCO Utilizing Transformer Coupling Technique

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Graduate Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University

Abstract— This paper introduces an 80-GHz voltage-controlled oscillator (VCO) based on a dual-core architecture. Each core is equipped with a capacitor-loaded transformer, and the two transformers are interconnected through switches. By manipulating these switches, the tank inductance can be adjusted, which enables the VCO to operate in three different frequency modes without degrading phase-noise performance. The design further employs a Class-D topology to boost its performance under sub-1V supply voltages and W-band frequency conditions. The presented VCO is fabricated in 40-nm CMOS process, with a core area of 0.057 mm2. Consuming 26.48 mW PDC under a 0.8-V supply, the Frequency tuning range (FTR) is 18.2 %. PN at 10-MHz offset is -111.68 dBc/Hz with a FoM of -175.6 dBc/Hz and FoMT of -180.6 dBc/Hz.

S07.3

A 0.5 V 2.4 GHz Digital PLL with a Sub-feedback Loop Technique

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This work presents a digital bang-bang phase-locked loop (BBPLL) for a low supply voltage application. The digital BBPLL uses a five-stage ring oscillator with a forward interpolator sub-feedback loop to obtain a higher output frequency at a low supply voltage. The proposed digitally controlled oscillator (DCO) uses a 4-bit second-order delta-sigma modulator (DSM) to improve the jitter performance and achieve a high timing resolution. The proposed digital BBPLL was implemented by the TSMC 90nm 1P9M CMOS process. This digital BBPLL can operate at the supply voltages of 0.5V. The chip area and core area are 550μm×550μm and 59μm×110μm, respectively. Measurement results show that the digital BBPLL achieves an operating frequency of 2.4 GHz at a supply voltage of 0.5V. The peak-to-peak jitter and RMS jitter of digital BBPLL were 23.46 ps (5.63%) and 2.68 ps (0.64%),

respectively. The power consumption was 283.4μW.

S07.4

A 28 Gb/s Clock and Data Recovery Circuit with Phase Interpolation for Bi-Directional Die-to-Die Communication

Yang Su, Shao-Chun Chuang, Ching-Yuan Yang
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This paper presents a 28 Gb/s clock and data recovery (CDR) circuit that employs phase interpolation to enable simultaneous bi-directional die-to-die communication. A 14 GHz low-jitter frequency synthesizer, based on a Type-II fourth-order phase-locked loop (PLL), is integrated to generate the high-frequency clock. The synthesizer utilizes a sampling loop filter to suppress control voltage ripple and reduce reference spurs. The proposed CDR achieves fine phase resolution through phase interpolation, ensuring robust clock alignment at high data rates. The circuit is implemented in a 28 nm CMOS process and operates at a 1 V supply voltage.

S07.5

An Area-Efficient SCR Design for RF ESD Protection

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A compact electrostatic discharge (ESD) protection circuit utilizing silicon-controlled rectifiers (SCRs) for radio frequency (RF) I/O pins is proposed and implemented in the TSMC 0.18-μm CMOS process. The design ensures robust ESD protection by enabling discharge through multiple paths between the I/O pins and power rails. To mitigate the parasitic capacitance introduced by the SCRs, an inductor is integrated for compensation. As a result,

the proposed circuit achieves comprehensive ESD protection while preserving high signal integrity and minimizing chip area, making it a highly efficient solution for high-frequency applications.