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SAB-based Continuous-time Delta-sigma Modulator with Random-skip Data-weighted Averaging Function

應用 SAB 濾波器與隨機亂數加權平均技巧之連續時間三角積分調變器

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作品摘要

無線通訊系統和人們的生活息息相關，在許多可攜式的應用中 (wireless sensor nodes、internet of things)，為了要延長電池壽命，降低無線通訊系統接收機的功率消耗一直都是一個重要的議題。在接收機架構中，類比數位轉換器 (analog-to-digital converter，ADC) 扮演著一個很重要的角色，因此，類比數位轉換器的頻寬、功率消耗及解析度都深深地影響著接收機的效能。此外，在類比數位轉換器架構的選擇上，考量接收機整體的性能，連續時間三角積分調變器 (CTDSM) 由於具有 inherent anti-alias filtering 的特性，前端濾波器的規格需求可以因此降低，加上可以達到相對高的解析度，因此，CTDSM 經常地被使用在低功耗接收機。隨著現今通信協定對於頻寬需求的增加，許多研究也因此著墨在如何在增加頻寬的同時降低功率消耗。取樣頻率也隨之提升。

在 CTDSM 設計上，仍然有持續進步的空間。首先，信號頻寬增加，用於迴路濾波器中的運算放大器 gain bandwidth 需求也會跟著提升，運算放大器需要消耗更大的功率來符合設計規格，第二、取樣頻率增加，CTDSM 中的量化器也需要操作在更高的頻率，因此量化器中的比較器頻寬也需要提高，縮短量化器所貢獻的電路延遲，避免系統的不穩定，第三、迴路延遲，整個 CTDSM 的信號路徑上包含了迴路濾波器、量化器、DWA 電路以及 DAC 電路，這些電路都會貢獻相當程度的電路延遲，而過多的電路延遲，會使得 CTDSM 的穩定度受到影響，進而有震盪的風險，這樣的現象在高速的應用中尤其嚴重。為了使 CTDSM 能夠容忍比較大的迴路延遲，保持系統穩定度，CTDSM 系統需要一個額外的延遲迴路補償路徑 (excess loop delay compensation path，ELDC path)，此路徑是將調變器輸出數位信號回授至量化器的輸入。為了實現此一補償路徑，電路系統需要額外的運算放大器實現加法電路以及回授 DAC 電路，這些電路皆需要消耗相當的功耗以及硬體。第四、數位類比轉換器中 mismatch 的非理想效應，通常會貢獻額外的 harmonic tones，進而使調變器的線性度變差，為了要強化 DAC 的線性度，通常會在調變器的回授路徑加入 data weighted averaging (DWA) 電路，將回授數位碼轉換成 barrel shifting 的形式，達到消除 DAC mismatch 的目的。此外，為了減少 DWA 造成的延遲並同時解決比較器輸入不匹配的問題，DWA 的機制改由旋轉比較器的準位電壓來實現。然而，在考量到數位類比轉換器輸出的寄生電容及放大器的輸入不匹配時，使用 DWA 會產生一些額外的第二諧波失真。圖中是一個具備 ELDC path 的 CTDSM 系統。

見附圖

針對上述的各種問題，此作品提出了以下概念，來降低功耗並同時達到高解析度、寬頻的需求。

- 在高階數的 CTDSM 中，此作品有效地重複使用積分器電流及硬體，在不影響到目標規格下，降低系統功耗以及電路複雜度。
- 將迴路延遲補償路徑融入積分器中，將此路徑的硬體及功率消耗最小化。
- 將時域概念融入量化器中，有效將低量化器的設計複雜度。
- 提出一個具有 random skipping 功能的 DWA(Data weighted averaging)，解決回授路徑的線性度問題。

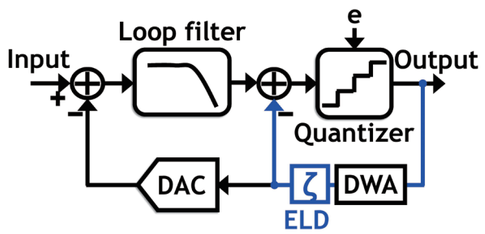

圖 1 / 連續時間三角積分調變器架構

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於 2001 取得美國加州大學洛杉磯校區（UCLA）博士學位，曾任職於博通（Broadcom Corporation）參與類比 / 射頻 / 混合訊號電路設計，並開發無線傳輸系統。2004 年加入臺灣大學電子工程學研究所擔任助理教授，並於 2009 年獲得臺大教學傑出獎，2011 年升任教授。

研究領域

無線通訊積體電路、頻率合成器、三角積分調變器、介面感測電路、電源管理電路。

Abstract

Wireless communications are widely associated with human daily life. For portable application, to lower down the power consumption of the wireless transceiver is the key point to prolong the battery life and friendly usage. Considering a receiver with a general topology, a key component is the analog-to-digital converter. The performance of the receiver is highly depending on the bandwidth, power consumption and resolution of the adopted data converter. There are many different types of data converters which include flash data converter, successive approximation data converter, pipeline data converter and delta-sigma modulator. Among the above architectures, the inherent anti-alias filtering property of the continuous-time delta-sigma modulator (CTDSM) can relax the design requirement of the previous stage filter. Benefiting from this trait, the CTDSM becomes a popular candidate for a low power receiver. However, there are still some design considerations and plenty of space for improvement on the wideband CTDSM. Nowadays, lots of publications still work on this field to further lower down the power consumption and extend the bandwidth of the next generation communication technology.

In a wideband low-power CTDSM design, there are several issues needed to be addressed. First of all, as the signal bandwidth increase, the gain bandwidth requirement on operational amplifier also increases. To meet the targeting bandwidth, more power consumption is necessary. The second issue is high sampling frequency. To keep the same resolution, the sampling frequency is increased with signal bandwidth. In other word, the operation frequency of the internal quantizer is therefore increased. Hence, the latency induced by the comparators need to be reduced to maintain the stability of modulator. The third issue is excess loop delay issue. The CTDSM system is consisted of loop filter, quantizer and feedback in a closed-loop manner. The latency induced by internal blocks would result in instability in high speed applications. Typically, in order to keep the implemented modulator stable, the input signal of the quantizer should be digitized and feedback to the input of the loop filter within half clock period. That's to say, the latency contributed by the loop quantizer and DWA logic should be shrank into half clock cycle (0.5/fs). Furthermore, in high speed application, the half clock cycle delay will lead to instability or performance degrade of the modulator. In order to accommodate the delay, an additional excess loop delay (ELD) compensation path is applied to feedback the modulator output to the quantizer input with a half clock cycle delay to guarantee sufficient phase margin for high speed CTDSM. The ELD compensation path is usually implemented with an additional feedback DAC and additional summer which increase additional power consumption and hardware. The fourth issue is mismatch issue. In multi-bit feedback DACs, the mismatch of DAC cells usually manifest itself as harmonic tones. DWA (Data weighted averaging) function is a well-known technique to address the non-linearity of DAC cells by randomizing the mismatch. Meanwhile, in order to minimize the latency induced by DWA logic and also mitigate the offset voltage of the comparators, DWA function is realized by rotating the reference voltages according to the output thermometer codes in flash-based quantizers. In this manner, the comparators have whole half cycle for quantization. However, in the presence of parasitic capacitance on DAC cells and mismatch on DAC switches, the signal-dependent pattern of 1st-order DWA function induces 2nd-order distortion and degrades the SNDR. The figure shows a typical CTDSM which is consisted a high order loop filter, a multi-bit quantizer, a multi-bit feedback DAC and ELD compensation path.

To address the aforementioned issues. This design proposes several techniques to achieve a power-efficient CTDSM with wide signal bandwidth and high resolution.

- Propose a SAB-based loop filter and apply it to a high-order CTDSM. In this manner, both power consumption and hardware complexity of the modulator can be reduced.
- Merge the ELD compensation path with SAB-based loop filter. As follows, the design effort on this compensation path is minimized.
- Implement a hybrid voltage-domain and time-domain quantizer to reduce the number of comparators.
- Propose a DWA function with inherent random skipping function to resolve the linearity issue of feedback DAC.