A 400MHz 10Mbps D-BPSK Receiver with a Reference-less Dynamic Phase-to-Amplitude Demodulation Technique

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Abstract

A 400MHz 10Mbps differential BPSK (D-BPSK) receiver (RX) is presented. This RX adopts a proposed reference-less dynamic phase-to-amplitude demodulation scheme, which converts signal phase transition to distinct amplitude variation. The proposed RX can support a data rate up to 10Mbps. It achieves -63dBm sensitivity at 0.1% BER and draws 1.77mW in 0.18μm CMOS.

Introduction

Short-range medium-to-high data rate wireless telemetry is required in many biomedical applications. Due to limited energy source, an energy efficient RX is highly desired. Considering spectral efficiency, SNR, and robustness of the wireless link, PSK modulation schemes [1-3] are favored. However, detection of absolute phase information [4] complicates the circuit design. In this work, a dynamic phase-to-amplitude conversion technique based on injection locking is proposed to detect the phase transition of a D-BPSK signal without using a power hungry PLL and a reference crystal oscillator. The presented receiver supports a data rate of 10Mbps and achieves a sensitivity of -63dBm at 0.1% BER. Operated from a 0.9V supply, the RX draws 1.77mW.

RX with Dynamic Phase-to-Amplitude Scheme

Fig. 1 shows the block diagram of the proposed RX. The D-BPSK RX consists of an LNA, an LC-DCO, an envelope detector, a data slicer, and an RZ-to-NRZ converter. The input RF signal amplified by the LNA is injected to the LC-DCO. If the input signal undergoes an 180^0 phase change, the DCO is perturbed and it reacts with a transient oscillation envelope variation in the process of reestablishing injection lock. This distinct pattern of momentary oscillation envelope variation is captured and manipulated by the data slicer and RZ-to-NRZ converter to demodulate the D-BPSK signal. In the proposed dynamic phase-to-amplitude demodulation scheme, a PLL is not required to precisely set the DCO frequency or accurately detect the absolute phase. A coarse DCO frequency tuning is sufficient. The DCO is designed with a 9bit frequency tuning and the tuning resolution is about 250kHz.

The operation principle of the proposed D-BPSK demodulator is introduced in Fig. 2. As depicted in the phasor plot, when the LC-DCO is injection locked, the injection current vector, I_{INJ}, is approximately in phase with the total current (I_t) flowing into the LC tank of DCO. However, when the phase of the input injection signal changes by 180^0, the magnitude of vector I_t is reduced owing to the vector reversal of I_{INJ}, which leads to reduction of oscillation amplitude ($V_{OSC}(t)$). As the frequency of the injection signal is unchanged, the DCO will acquire locking and return to the injection-locked state again. $V_{OSC}(t)$ will settle to its initial amplitude, i.e., the amplitude before 180^0 phase change. Due to such behavior, the envelope detector output mimics a return-to-zero (RZ) characteristic. The differentially encoded input data can be decoded by performing an RZ-to-NRZ conversion. The associated waveforms are illustrated in the bottom of Fig. 2.

Circuit Implementation

The RF front-end circuit implementations are shown in Fig. 3. A differential common-source LNA is realized in considering lower noise and immunity to common-mode noise. To provide enough gain, inductive loading is preferred. However, as the 400MHz LC-DCO already uses a large on-chip passive inductor, the LNA load inductors are implemented with active circuits for area consideration. Q-enhancement circuit is added to boost the LNA gain. The LNA outputs are converted to currents via the transconductor stage (M_1/M_2), and the currents are injected to the DCO for injection locking. The total peak gain provided by the input matching, LNA, and Q-enhancement technique is about 50dB. The gain can be controlled by adjusting the bias currents. The LNA along with the transconductors determines the injection strength which affects the RX sensitivity, and must be designed carefully. The LC-DCO frequency, controlled by a 9bit capacitor array, ranges from 380MHz to 500MHz.

Fig. 4 shows the baseband circuits including an envelope detector, a data slicer, and an RZ-to-NRZ converter. The envelope detector is realized as an active rectifier. The envelope detector output feeds the data slicer to generate the raw data. Since the envelope peak and valley levels will vary due to PVT variations, the threshold voltage of the slicer must be adaptively adjusted. This threshold voltage is generated by measuring the envelope peak and valley voltages and then taking the average of these two. The recovered data at slicer output are in RZ format as described in Fig. 2 and are converted to the NRZ form. The RZ-to-NRZ converter (not shown in Fig. 4) is implemented with a sampler operating at the data rate speed. The RX power consumption is dominated by LNA and LC-DCO, which draws 0.79mW and 0.84mW, respectively. The remaining circuits operate at the data rate speed and they consume much less power.

Experimental Results

Fig. 5 shows the RX performance measured at a carrier frequency of 435MHz. The displayed waveforms include the transmitted TX data, envelope detector output, and RX decoded data. Distinct pattern of envelope variation as described in Fig. 2 is observed. The measured BER vs. RX input power is shown in Fig. 6. For 10Mbps data rate at 0.1% BER, the sensitivity is -63dBm; the sensitivity is improved to -68dBm and -71dBm for 5Mbps and 2.5Mbps data rate, respectively. Fig. 7 shows the RX sensitivity vs. frequency offset between input RF frequency and free-running DCO frequency. The blocker rejection capability is shown in Fig. 8. The result shows that an offset of 250kHz (LC-DCO frequency resolution) results in about 0.4dB sensitivity loss. Fig. 9 illustrates RX power consumption vs. sensitivity. Power consumption is controlled by adjusting the bias currents of LNA and LC-DCO. If the sensitivity requirement is relaxed, power consumption of RX can be lowered.

The RX is fabricated in TSMC 0.18μm CMOS process. Fig.

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10 shows the chip micrograph. The proposed RX is fully integrated; it employs an on-chip inductor for LC-DCO and 2 on-chip source inductors (L_S of Fig. 3) for LNA. Fig. 11 illustrates the receiver benchmark, including energy efficiency and sensitivity. Table 1 summarizes the experimental results and compares with other similar low-power PSK RX works. Compared to [1] and [2], the proposed RX consumes more power; but it supports a higher data rate with significantly improved sensitivity. Take sensitivity, data rate and power consumption into consideration, the RX achieves an FOM more than 160 under various data rate operation.

Acknowledgement

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References

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[2] H. Yan et al., *IEEE T-MTT*, vol.59, pp. 1339-1349, May 2011.

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[4] W. Z. Chen et al., *IEEE TCAS-1*, vol. 59, pp. 505-514, Mar. 2012.

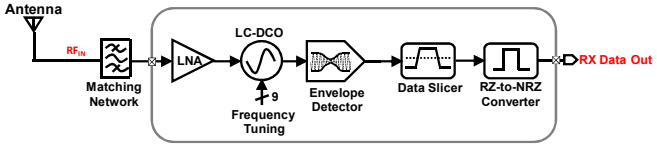

Fig. 1 Architecture of the proposed D-BPSK RX.

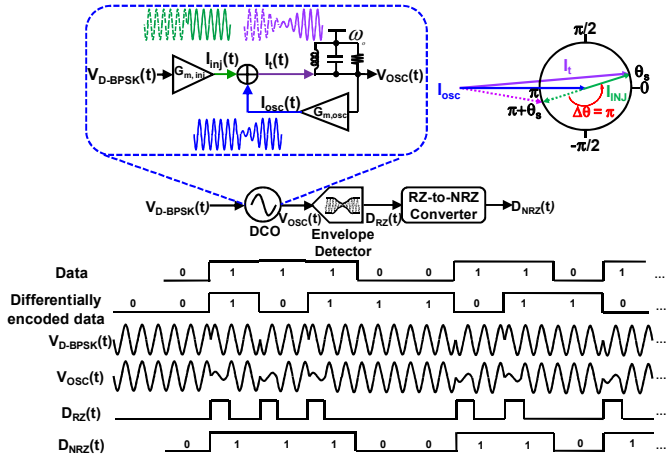

Fig. 2 Concept of the proposed D-BPSK demodulation.

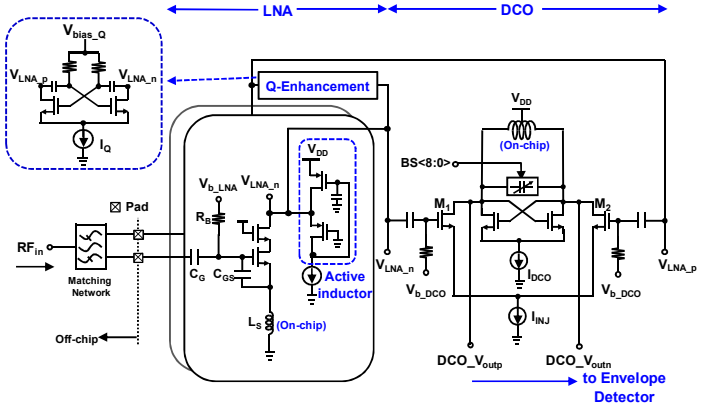

Fig. 3 Simplified RF front-end schematic.

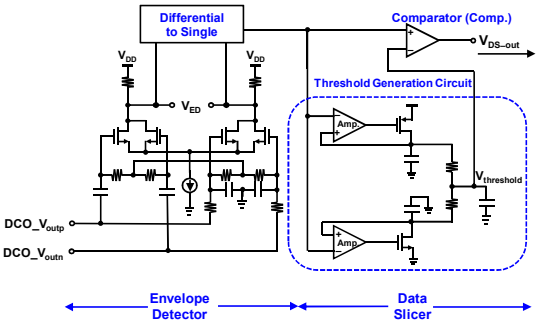

Fig. 4 Simplified baseband schematic.

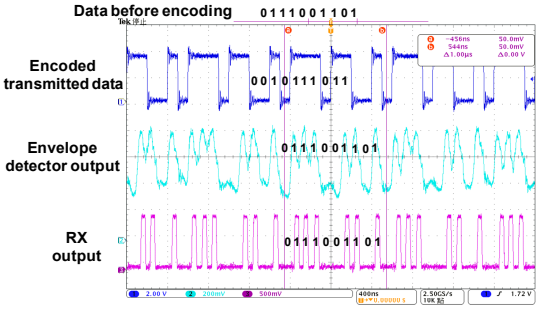

Fig. 5 Data transient measurement.

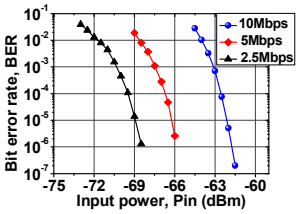

Fig. 6 BER vs. input power.

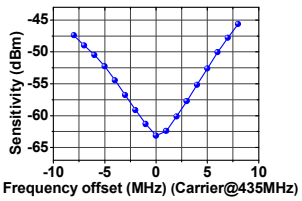

Fig. 7 Sens. vs. freq. offset.

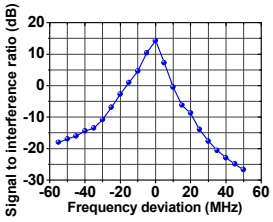

Fig. 8 Blocker rejection.

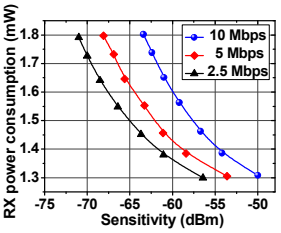

Fig. 9 RX power vs. Sens.

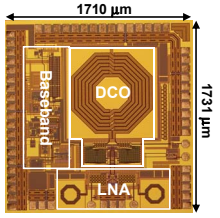

Fig. 10 Chip micrograph.

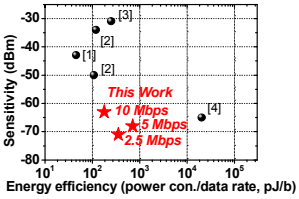

Fig. 11 Receiver benchmark.

Table I Performance summary and comparison

	This Work	[1]	[2]	*[3]	[4]
Technology	CMOS 0.18 µm	CMOS 65 nm	CMOS 90 nm	CMOS 90 nm	CMOS 0.18 µm
Supply (V)	0.9	1.2	1.2	0.8	1.8
Modulation	D-BPSK	BPSK	BPSK	BPSK	QPSK
Freq. Band (MHZ)	435	750	300 / 900	19000	2400
Power Con. (mW)	1.77	0.228	0.12 / 0.216	2.5	20.4
Data Rate (Mbps)	2.5 / 5 / 10	5	1 / 2	10	1
Sensitivity (dBm)	-71 / -68 / -63	-43	-34 / -50	-31	-65
**FoM	163 / 163 / 161	146	133 / 150	127	142

*Demodulator only
**FoM = – Sensitivity – 10 * log (Power Con. / Data Rate)